voltages by selecting different values of SEC. An increase of SEC results in a proportional increase of the corresponding holding voltage. As such, an advantageous feature of this embodiment is that semiconductor devices having different voltage ratings (e.g., 20V, 30V, 40V) may be fabricated based upon the same basic structure by selecting different values of SEC.

[0030] FIG. **4** illustrates a simplified cross-sectional view of an ESD protection structure **400** in accordance with an alternate embodiment. As shown in FIG. **4**, the first high voltage P type implanted region **108** is disposed below the first P+ region **102**. However, the second high voltage P type implanted region **110** is not disposed in the ESD protection structure **400**. The first high voltage P type implanted region **108** has the same conductivity type as the first P+ region **102**, so that the first high voltage P type implanted region **108** may extend the first P+region **102** into a deeper level. This helps to provide a different holding voltage characteristic different from a conventional bipolar PNP transistor.

[0031] FIG. **5** illustrates an equivalent circuit diagram of the ESD protection structure **400** illustrated in FIG. **4**. An ESD protection circuit **500** includes a bipolar PNP transistor **502** having an emitter **504**, a base **510**, a collector **506** and a resistor **508**. As shown in FIG. **4**, the first high voltage P type implanted region **108** and the first P+ region **102** form the collector **506**. The emitter **504** is formed by the second P+ region **104**. The resistor **508** represents the parasitic resistance in the HVNW **106** (not shown but illustrated in FIG. **4**). Similar to the ESD protection circuit **200** described with respect to FIG. **2**, the ESD protection circuit **500** can provide an ESD current path once the voltage across the emitter **504** and the collector **506** exceeds the breakdown voltage of the bipolar PNP transistor **502**.

[0032] FIG. **6** illustrates a simplified cross-sectional view of an ESD protection structure **600** in accordance with another embodiment. As shown in FIG. **6**, the second high voltage P type implanted region **110** is disposed below the second P+ region **104**. However, the first high voltage P type implanted region **108** is not disposed in the ESD protection structure **600**. The second high voltage P type implanted region **110** has the same conductivity type as the second P+ region **104**, so that the second high voltage P type implanted region **110** may extend the second P+ region **104** into a deeper level. This helps to provide an ESD current path having a different characteristic from the conventional PNP transistor.

[0033] FIG. **7** illustrates an equivalent circuit diagram of the ESD protection structure **600** illustrated in FIG. **6**. An ESD protection circuit **700** includes a bipolar PNP transistor **702** having an emitter **704**, a base **710**, a collector **706** and a resistor **708**. As shown in FIG. **6**, the second high voltage P type implanted region **110** and the second P+ region **104** form the emitter **704**. The collector **706** is formed by the first P+ region **102**. The resistor **708** represents the parasitic resistance in the HVNW **106** (not shown but illustrated in FIG. **6**). Similar to the ESD protection circuit **200** described with respect to FIG. **2**, the ESD protection circuit **700** can provide an ESD current path once the voltage across the emitter **704** and the collector **706** exceeds the breakdown voltage of the bipolar PNP transistor **702**.

[0034] FIG. **8** illustrates an integrated circuit level ESD protection diagram. An integrated circuit chip **800** has a VDD pad **808**, an I/O pad **806** and a VSS pad **804**. Internal circuits **802** are coupled to the VDD pad **808** and VSS pad **804**. The internal circuits **802** further include an input coupled to the I/O pad **806**. The ESD protection circuit **200** is coupled between the I/O pad **806** and the VSS pad **804**. It should be noted that the ESD protection circuit **200** is provided for illustrative purpose only. The ESD protection circuit between the I/O pad **806** and the VSS pad **804** may be any of the ESD protection circuits **200**, **500** and **700** shown in FIG. **2**, FIG. **5** and FIG. **7** respectively.

[0035] When an ESD event occurs between the I/O pad **806** and the VSS pad **804**, the ESD protection circuit **200** conducts the ESD current, and the turn-on of an ESD protection circuit (e.g., the ESD protection circuit **200**) clamps the voltage between the I/O pad **806** and the VSS pad **804** below the maximum voltage to which the internal circuits **802** are specified, so that the internal circuits **802** coupled between the I/O pad **706** and the VSS pad **705** are protected. An advantageous feature of the described circuit level ESD protection is the ESD protection circuit provides a bypass for ESD current to flow so that the internal circuits are protected.

[0036] It should be noted that the ESD protection circuit **200** may be coupled between the VDD pad **808** and the VSS pad **804** as indicated by the dashed line in FIG. **8**. When an ESD event occurs between the VDD pad **808** and the VSS pad **804**, the conduction of the ESD protection circuit clamps the voltage between the VDD pad **808** and the VSS pad **804**, so that the internal circuits such as internal circuits **802** are protected. In short, the connection of the ESD device **200** in FIG. **8** is merely an example, which should not unduly limit the scope of the claims. One skilled in the art will recognize many variations, alternatives, and modifications.

[0037] FIG. **9** illustrates a further ESD protection scheme by employing a plurality of ESD protection circuits in series connection between an I/O pad and a VSS pad. Similar to FIG. **8**, FIG. **9** includes an integrated circuit **800**, a VDD pad **808**, an I/O pad **806**, a VSS pad **804** and internal circuits **802**. However, FIG. **8** further includes a series connection of ESD protection circuits electrically coupled to the I/O pad **806** and the VSS pad **804**. In high voltage applications, a single ESD protection circuit such as the ESD protection circuit **200** shown in FIG. **8** may not provide a reliable ESD protection. By contrast, a plurality of ESD protection circuits **200** in series connection may provide an adjustable ESD protection breakdown point as well as an adjustable ESD protection holding voltage.

[0038] In FIG. **9**, if an ESD event occurs, a voltage spike is applied between the I/O pad **806** and the VSS pad **804**. The series-connected ESD protection circuits may turn on nearly simultaneously. Each ESD protection circuit provides an ESD protection holding voltage. The sum of all series-connected ESD protection circuits' breakdown voltages clamps the I/O pad's voltage **806** to a level below the maximum rating voltage of the internal circuits **802**, so that the internal circuits **802** are protected.

[0039] As described above with respect to FIG. **8**, placing an ESD device between the I/O pad **806** and the VSS pad **804** in FIG. **9** is merely an example. One skilled in the art will recognize many variations, alternatives, and modifications, such as connecting the ESD device between the VDD pad **808** and the VSS pad **804** as indicated by the dashed line in FIG. **9**.

[0040] In the embodiments, by controlling the distance between two high voltage P type implanted regions, the ESD protection device can have an adjustable threshold voltage for